CLAIMS

1. A microprocessor structure for performing a discrete wavelet transform operation, said discrete wavelet transform operation comprising decomposition of an input signal vector comprising a number of input samples, over a specified number of decomposition levels j, where j is an integer in the range 1 to J, starting from a first decomposition level and progressing to a final decomposition level, said microprocessor structure having a number of processing stages, each of said stages corresponding to a decomposition level j of the discrete wavelet transform and being implemented by a number of basic processing elements, the number of basic processing elements implemented in each of said processing stages decreasing by a constant factor at each increasing decomposition level j.

2. A microprocessor structure according to claim 1, wherein the input signal vector comprises $r \times k^m$ input samples, r, k and m being non-zero positive integers and the number of basic processing elements implemented in each of said processing stages of said microprocessor structure decreases by a factor of k from a decomposition level j to a decomposition level j + 1.

3. A microprocessor structure according to claim 2 the microprocessor structure being arranged to process all of said $r \times k^m$ input samples of said input vector in parallel.

4. A microprocessor structure according to claim 2 further comprising $r \times k^m$ inputs arranged to receive all of said $r \times k^m$ input samples of said input vector in parallel.

5. A microprocessor structure according to claim 2 wherein the number of said basic processing elements in the first processing stage is equal to $r \times k^{m-1}$.

6. A microprocessor structure according to claim 2, wherein each basic processing element of each processing stage has a predetermined number of in-

puts and is arranged to perform a set of k inner product operations between k sets of coefficient values and a set of input values received in parallel at said predetermined number of inputs, the number of said inputs, the number of said coefficient values in a set and the number of said input values received in parallel each being equal to a filter length L used to form said k inner products, said basic processing element further comprising k outputs, each output arranged to output an output value corresponding to a result of one of said set of k inner products performed between one of said k sets of coefficient values and said set of input values.

7. A microprocessor structure according to claim 2, wherein each basic processing element of each processing stage has a predetermined number of inputs and is arranged to perform a set of k inner product operations between k sets of coefficient values and a set of input values received in parallel at said predetermined number of inputs, the number of said inputs and the number of said input values received in parallel being equal to a filter length L_{long}, where L_{long} is the largest number of coefficient values used to form any of said k inner products, said basic processing element further comprising k outputs, each output arranged to output an output value corresponding to a result of one of said set of k inner products performed between one of said k sets of coefficient values and said set of L input values.

8. A microprocessor structure according to claim 1, wherein each basic processing element of each processing stage has a predetermined number of inputs and is arranged to perform two inner products between two sets of coefficient values and a set of input values received in parallel at said L inputs, a first of said two inner products representing a low-pass filtering operation and a second of said two inner products representing a high-pass filtering operation, the number of said inputs, the number of said coefficient values and the number of said input values received in parallel being equal to a filter length L used to form said two inner products, said basic processing element further comprising two outputs, a first output arranged to output a low-pass

filtered output value corresponding to a result of the low-pass filtering operation performed on said set of input values, and a second output being arranged to output a high-pass filtered output value corresponding to a result of the high-pass filtering operation performed on said set of input values.

9. A microprocessor structure according to claim 2, wherein at least one of the processing stages 2 to J, further comprises a data routing block arranged to receive a specified one of said k outputs values from each of the basic processing elements of an immediately preceding processing stage j - 1, said routing block being further arranged to group said specified ones of said k output values into sets of L output values and to supply said sets of L output values in parallel to the inputs of the basic processing elements of processing stage j, such that each basic processing element of processing stage j receives a predetermined set of L output values obtained from said immediately preceding processing stage j - 1.

10. A microprocessor structure according to claim 1, wherein at least one of the processing stages 2 to J, further comprises a routing block arranged to receive low-pass filtered output values from each of the basic processing elements of an immediately preceding processing stage j - 1, said routing block being further arranged to group said low-pass filtered output values into sets of L low-pass filtered output values and to supply said sets of L low-pass filtered output values in parallel to the inputs of the basic processing elements of processing stage j, such that each basic processing element of processing stage j receives a predetermined set of L low-pass filtered output values obtained from said immediately preceding processing stage j - 1.

11. A microprocessor structure according to claim 1, wherein the processing stage corresponding to said first decomposition level further comprises a routing block arranged to receive said $r \times k^m$ input samples of said input vector, said routing block being arranged to group said $r \times k^m$ input samples into sets of L input samples and to supply said sets of L input samples in parallel

to the inputs of the basic processing elements of the first processing stage, such that each basic processing element of the first processing stage receives a predetermined set of L input samples.

12. A microprocessor structure according to claim 1, wherein the processing stage corresponding to said first decomposition level further comprises a routing block arranged to receive 2^m input samples of said input vector, said routing block being arranged to group said 2^m input samples into sets of L input samples and to supply said sets of L input samples in parallel to the inputs of the basic processing elements of the first processing stage, such that each basic processing element of the first processing stage receives a predetermined set of L input samples.

13. A microprocessor structure according to claim 1 wherein each basic processing element of each processing stage has a predetermined number of inputs and is arranged to perform two inner product operations between two sets of coefficient values and a set of input values received in parallel at said predetermined number of inputs, the number of said inputs, the number of said coefficient values in a set and the number of said input values received in parallel each being equal to a filter length L used to form the two inner products, said basic processing element further comprising two outputs, each output arranged to output respective ones of the two inner products, the microprocessor structure further comprising a data routing block arranged to receive pairs of inner products from the basic processing elements which performs a perfect unshuffle operation to group together inner products from like filtering operations from each of the processing elements.

14. A microprocessor structure according to claim 2 wherein each basic processing element of each processing stage has a predetermined number of inputs and is arranged to perform k inner product operations between k sets of coefficient values and a set of input values received in parallel at said predetermined number of inputs, the number of said inputs, the number of said

coefficient values in a set and the number of said input values received in parallel each being equal to a filter length L used to form the k inner products, said basic processing element further comprising k outputs, each output arranged to output respective ones of the k inner products, the microprocessor structure further comprising a data routing block arranged to receive k inner products from the basic processing elements which performs a stride permutation to group together inner products from like filtering operations of each of the processing elements.

15. A microprocessor structure according to claim 1, wherein a discrete wavelet transform result to an arbitrary decomposition level j, is formed by a vector constructed from output values from a high-pass filtering operation and a low-pass filtering operation at a processing stage corresponding to the arbitrary decomposition level j and output values from high-pass filtering operations of all preceding processing stages.

16. A microprocessor structure according to claim 2, wherein the microprocessor structure comprises at least one core processing unit, said core processing unit comprising k^{j-1} basic processing elements at each processing stage j.

17. A microprocessor structure according to claim 16, wherein each basic processing element of each processing stage has a predetermined number of inputs and is arranged to perform a set of k inner product operations between k sets of coefficient values and a set of input values received in parallel at said predetermined number of inputs, the number of said inputs, the number of said coefficient values in a set and the number of said input values received in parallel each being equal to a filter length L used to perform said k inner product operations, each basic processing element further comprising k outputs, each output arranged to output an output value corresponding to a result of one of said k inner product operations performed between one of said k sets of coefficient values and said set of input values.

18. A microprocessor structure according to claim 16, wherein at least one of said processing stages 2 to J further comprises a data routing block arranged to receive said k output values from each of the basic processing elements of an immediately preceding processing stage j – 1, said routing block being further arranged to group together selected ones of said k output values into sets of L output values and to supply said sets of L output values in parallel to the inputs of the basic processing element of processing stage, in such a way that each basic processing element of processing stage j receives a predetermined set of L output values received from said immediately preceding processing stage j – 1.

19. A microprocessor structure according to claim 16, wherein the processing stage corresponding to the first decomposition level further comprises a routing block arranged to receive said consecutive sub-vectors i comprising k^j input samples, said routing block being arranged to form said k^j input samples into sets of L input samples, by arranging the sub-vectors i to be exactly divisible into said sets of L by appending a number of samples from an immediately subsequent sub-vector i + 1, said routing block being further arranged to supply said sets of L input samples in parallel to the inputs of the basic processing elements of the first processing stage, such that each basic processing element of the first processing stage receives a predetermined set of L input samples.

20. A microprocessor structure according to claim 16, wherein said microprocessor is arranged to receive sub-vector comprising k^j input samples of said r x k^m input samples of said input vector.

21. A microprocessor structure according to claim 20 which is arranged to receive the k^j input samples in parallel.

22. A microprocessor structure according to claim 20, wherein the first processing stage of the microprocessor structure is arranged to receive said vector of r x k^m input samples progressively in time, as consecutive sub-vectors.

23. A microprocessor structure according to claim 22 wherein at least one processing stage is arranged to process a sub-vector i in a first time period which includes at least one sample from a sub-vector i + 1 in a second time period immediately consecutive to the first time period.

24. A microprocessor structure according to claim 23 wherein the at least one processing stage is arranged to process the sub-vector i appended with L/2 samples from the sub-vector i + 1.

25. A microprocessor structure according to claim 1, wherein each basic processing element is arranged to execute a basic operating cycle in a period of time which is substantially the same for all basic processing elements.

26. A microprocessor structure according to claim 19 further comprising a shift register arranged to form the sub-vectors from the vector of input samples.

27. A microprocessor structure according to claim 1, wherein all of said basic processing elements are implemented to perform identical operations.

28. A microprocessor structure according to claim 18, wherein the number of samples appended to sub-vector i is L / 2.

29. A microprocessor structure according to claim 16, wherein each basic processing element of each processing stage has a predetermined number of inputs p and is arranged to perform a set of k inner product operations between k sets of coefficient values and a set of input values, the total number of said input values in a set and the number of coefficient values in a set being equal to L, where L is selectable in a range from 1 to L_{max} , said basic

processing element being further arranged to receive a set of p input values in parallel at said p inputs at a given time and to perform a sub-set of inner product operations comprising k inner product operations between p coefficient values and said p input values in a given operating period.

30. A microprocessor structure according to claim 29, wherein each basic processing element is arranged to receive a set of p input values at consecutive operating periods.

31. A microprocessor structure according to claim 29, wherein each basic processing element further comprises k outputs, each output arranged to output an output value corresponding to a result of one of said k inner product operations performed between one of said k sets of coefficient values and said set of input values.

32. A microprocessor structure according to claim 29, wherein at least one of the processing stages 2 to J, further comprises a data routing block arranged to receive said k output values from each of the basic processing elements of an immediately preceding processing stage j – 1, said routing block being further arranged to group specified ones of said k output values into sets of L output values and to supply said sets of L output values in consecutive groups of p values in parallel to the p inputs of the basic processing elements of processing stage j at successive operating periods.

33. A microprocessor structure according to claim 29, wherein the processing stage corresponding to the first decomposition level further comprises a routing block arranged to receive said consecutive sub-vectors i comprising k^j input samples, said routing block being arranged to form said k^j input samples into sets of L input samples, by arranging the sub-vectors i to be exactly divisible into said sets of L by appending a number of samples from an immediately subsequent sub-vector i + 1, said routing block being further arranged to supply said sets of L in consecutive groups of p values in parallel

to the p inputs of the basic processing elements of the first processing stage at successive operating periods.

34. A microprocessor structure according to claim 1, wherein at least one basic processing element is functionally connected to at least one other basic processing element of the same processing stage.

35. A microprocessor structure according to claim 29, wherein at least one basic processing element is functionally connected to at least one other basic processing element of the same processing stage j.

36. A microprocessor structure according to claim 29, wherein at least a first basic processing element of a processing stage j is arranged to receive an input from a second basic processing element in the same processing stage j.

37. A microprocessor structure according to claim 36, wherein said input from said second basic processing element in the same processing stage is a set of p values representing p intermediate results of inner product operations performed in said second basic processing element in an earlier operating period and said first basic processing element is arranged to use said set of p intermediate results in performing its inner product operations in a current operating period.

38. A microprocessor structure according to claim 37, wherein said p intermediate results are received in parallel at said first basic processing element.

39. A microprocessor structure according to claim 37, wherein said first basic processing element receives a set of p input values from said second basic processing element at each successive operating period, after an initial first operating period.

40. A microprocessor structure according to claim 1, integrated in a single device with a second microprocessor structure for performing a discrete wavelet transform, said second microprocessor structure being arranged to perform at least one further decomposition level in addition to said final decomposition level J.

41. A microprocessor structure according to claim 16, integrated in a single device with a second microprocessor structure for performing a discrete wavelet transform, said second microprocessor structure being arranged to perform at least one further decomposition level in addition to said final decomposition level J.

42. A microprocessor structure according to claim 29, integrated in a single device with a second microprocessor structure for performing a discrete wavelet transform, said second microprocessor structure being arranged to perform at least one further decomposition level in addition to said final decomposition level J.

43. A microprocessor structure according to claim 40, wherein said second microprocessor structure is arranged to perform a recursive pyramid algorithm.

44. A method of performing a discrete wavelet transform operation carrying out steps for implementation in the structure of claim 1.

45. A microprocessor structure according to claim 1, wherein the microprocessor structure comprises at least one core processing unit, said core processing unit arranged to perform a k_j-point wavelet transform operation.